Large Signal Bias-Dependent Modeling of PHEMTs by Pulsed Measurements

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***Abstract* — A bias-dependent large signal model and corresponding parameter extraction procedures are presented to characterize PHEMT transistors by pulsed measurements. Two nonlinear current sources and few additional parameters are used to model bias-dependence of the drain current. Results show that the method discussed in this letter can be applied to model the large signal behavior of PHEMTs from DC to RF at any bias points.**

I. Introduction

The advantages of measuring transistors by pulse and measurement systems have been discussed by many literatures [1] [2]. It has been observed that the pulsed measurement results are dependent on the bias points of the transistors [3][4][5], since transistors' trapping effect, channel resistance and temperature caused by the self-heating effect are bias-dependent. In [3], the bias dependence is taken as a function of power dissipation with an association time constant, and the drain current is simply normalized for heating by a function of average power. The trapping effect to the current is measure in [5] and modeled by two different gate voltage sources. One is the exact voltage enforced on the gate, and the other is a pseudo-backgate terminal voltage.

In the bias dependent model given in [4], the drain current is modeled by two nonlinear sources, one is bias independent, and the other is bias dependent which represents the difference between the DC and pulsed characteristics at every bias points. All the parameters in the resultant current model are functions of bias points. Similarly in the model presented in this letter, two nonlinear sources are used to model the drain current. However the model parameters are bias independent and only few additional parameters are introduced to couple the bias points into the current model equations.

This procedure is implemented to characterize PHEMTs processed in foundry, and the model is extracted successfully through the DC and RF data measured by the HP85108A pulsed system.

II. Summary of the bias-dependent modeling

A $8\times100um\times0.25um$ PHEMT on wafer from processed in foundry is measured to show the bias dependent behavior. Figure 1 gives the measured drain currents varying with bias points at drain and gate, the pulse voltages is fixed at $(-0.5V,3V)$ for gate and drain respectively.

The model given in this paper is developed from HP EEHEMT1. Figure 1 gives the equivalent circuit model to be used, in which $L_{G,D,S}$ and $R_{G,D,S}$ are the gate, drain, source parasitic inductances and resistances respectively. I_{GS} and I_{DS} are gate-source, gate-drain and drain-source currents respectively. C_{CGS} and C_{CGD} represent the gate charge model. R_{CGS} and R_{CGD} are used to model charging delay between the depleting region and the channel. C_{DS0} is the drain-source inter-electrode capacitance. As in [7], a current I_{DDS} associated with R_{DDS} and C_{DDS} are applied to model the trapping effect [10]. Since the trapping effect is dependent on the bias points while influence of instantaneous pulses is negligible [8], the bias dependent model can characterize the bias dependence of the trapping effect.

In the pulsed measurements, the device is biased at a fixed point, and very short pulses with pulse duration generally no more that few microseconds and duty cycle about 0.1% are enforced to the device. The bias voltages are represented by subscript B, and the pulse voltages are represented by subscript P. The bias dependent expression for the drain current model is give as

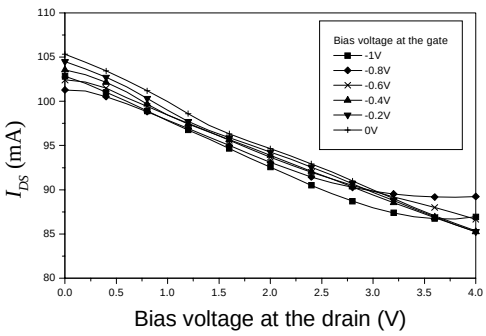

Figure 1 Drain current varying with the bias points when the pulse voltage is given at $(-0.5,3)V$.

$$I_{DS}\left(V_{GS}^{(P)},V_{DS}^{(P)};V_{GS}^{(B)},V_{DS}^{(B)}\right)=\left(I_{dso}-I_{comp}\right)\left(1+\mathrm{K}_a V_{DS}^{(S)}\right)\tanh\left(\alpha V_{DS}^{(S)}\right) \quad (1)$$

where α is constant to be determined, I_{dso} and I_{comp} are continuous through at least the second derivative everywhere. I_{comp} is a modification term to simulate the device compression behavior, and its expressions are ignored here. The expression of I_{dso} is given by a piece-wise function

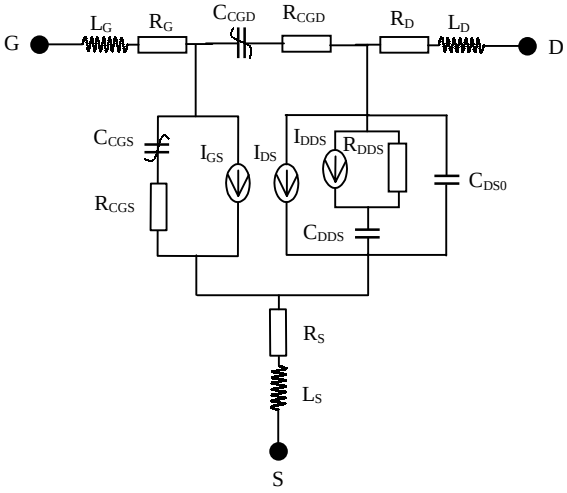

Figure.2 Equivalent circuit

If $V_{GS}^{(S)} > \left(V_{go}-V_{ch}\right)\left[1+\Gamma\left(V_{dso}-V_{DS}^{(S)}\right)\right]^{-1}+V_{ch}$,

$$I_{dso}=G_{m\max}\left[\begin{matrix}V_{GS}^{(S)}-0.5\left(V_{go}+V_{to}\right)\\+\Gamma\left(V_{GS}^{(S)}-V_{ch}\right)\left(V_{dso}-V_{DS}^{(S)}\right)\end{matrix}\right] \quad (2)$$

if $V_{GS}^{(S)} \le \left(V_{to}-V_{ch}\right)\left[1+\Gamma\left(V_{dso}-V_{DS}^{(S)}\right)\right]^{-1}+V_{ch}$,

$$I_{dso}=0 \quad (3)$$

otherwise,

$$I_{dso}=0.5G_{m\max}\left\{V_{GS}^{(S)}-V_{to}+\Gamma\left(V_{GS}^{(S)}-V_{ch}\right)\left(V_{dso}-V_{DS}^{(S)}\right)+\frac{V_{to}-V_{go}}{\pi}\sin\left[\pi\frac{V_{GS}^{(S)}-V_{go}+\Gamma\left(V_{GS}^{(S)}-V_{ch}\right)\left(V_{dso}-V_{DS}^{(S)}\right)}{V_{to}-V_{go}}\right]\right\} \quad (4)$$

where V_{go}, V_{ch}, V_{dso}, V_{ch}, V_{go}, V_{go}, Γ are constants to be determined, and

$$V_{DS,GS}^{(S)}=V_{DS,GS}^{(P)}+\lambda_{DS,GS}^{(0)}V_{DS}^{(B)}+\gamma_{DS,GS}^{(0)}V_{GS}^{(B)}+\sum_{n=1}^{N}\lambda_{DS,GS}^{(n)}\left(V_{DS}^{(P)}-V_{DS}^{(B)}\right)^n+\sum_{n=1}^{N}\gamma_{DS,GS}^{(n)}\left(V_{GS}^{(P)}-V_{GS}^{(B)}\right)^n \quad (5)$$

where $\left\{\lambda^{(n)},\gamma^{(n)},n=0,...,N\right\}$ are coefficients to be determined. It is found that $N=2$ can obtain accurate data fitting.

III. Procedures for Parameter Extraction

The Parasitic elements including $L_{G,D,S}$ and $R_{G,D,S}$ are extracted first. A nested optimization scheme [6] is used to tune the parasitic elements to fit the S-parameters measured as the gate voltage is swept in a wide interested region while the drain voltage is set at normal operating points. Before the optimization is applied, R_S is extracted and fixed by Yong-Long's method [7]. The predetermination of R_S speeds up the optimization process and improves the consistency of the solution. Above procedure can obtain robust results and good data fitting.

The initial values of $\{\lambda^{(n)},\gamma^{(n)},n=0,...,N\}$ are set to zero. Gate and drain currents are measured when the bias is fixed at a pinch-off point while the pulse voltages are swept. The model parameters are optimized. Then drain currents are measured when both the pulse and bias voltages are swept. Model parameters are tuned again simultaneously with $\{\lambda^{(n)},\gamma^{(n)},n=0,...,N\}$ to fit the measured data.

The charge model and dispersion model are extracted from the S-parameters measured in a wide frequency region with swept gate and drain voltages. To extract the dispersion model, R_{DDS} is set to a large enough value so that its contribution to the output conductance is negligible. And I_{DDS} is obtained though comparing the DC and AC drain current. The charge model is extracted from the gate capacitance directly obtained from the measured S-parameters.

IV. Measured and modeled results

Figure 3 compares the modeled drain current at two different bias points $(-0.5V,2V)$ and $(-0.5V,4V)$ with the measured data of the transistor with bias dependence depicted in figure 1. The agreement is good. Figure 4 gives the modeled and measured S parameters at $(-0.5V,3V)$. The results show that the bias dependent model obtained in this letter can be applied to model the transistor for large signal cases.

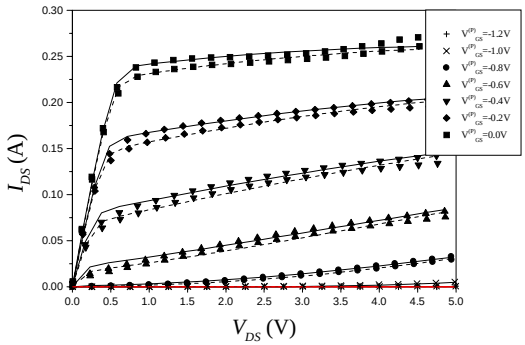

Figure 3 Measured and modeled drain currents at different bias points. The marks represent the measured data, the solid lines represent the modeled data for $2V$ drain bias voltage and the dashed lines represents the modeled data for $4V$ drain bias voltage. The gate bias voltage is fixed at $-0.5V$.

V. Conclusion

Pulsed measurements are applied to characterize the PHEMTs in this letter. The bias-dependent behavior is repeated accurately by large signal model obtained in this letter. Few parameters are required to depict the bias dependence.

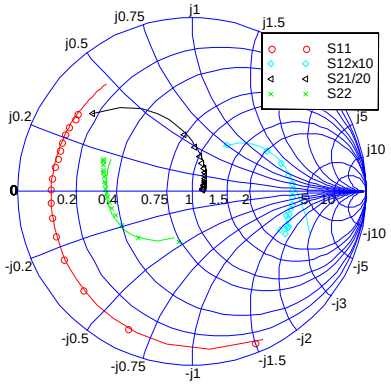

Figure 4 Measured and modeled S Parameters within $[1,21]GHz$ at $(-0.5,3)V$.

VI. References

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